IN THE CLAIMS

Please cancel claims 19, 20, 24, 29, 32, 33, 38, and 39 without prejudice. Claims 52-54 are new.

Please amend the following claims which are pending in the present application:

1-16. (Cancelled)

17. (Currently amended) A semiconductor package, comprising:

a substrate that includes a top surface and an exposed external opposite surface [defined by] including a first, inner region, a second, outer region around the inner region, and a third region that separates the first and second regions; and

a plurality of contacts including a first plurality of contacts and a second plurality of contacts, said first plurality of contacts located in a four-by-four matrix in the [second] first region, and said second plurality of contacts located in the [first] second region such that a smallest distance between adjacent contacts in both the first and second regions [is different] are smaller than a distance between the first and second regions, wherein the third region does not have any contacts located therein.

18. (Currently amended) The semiconductor package of claim 17, wherein the smallest distance between adjacent contacts in the first region are equal to the

smallest distance between adjacent contacts in the second region is smaller than the distance between the first and second regions.

19. (Cancelled)

20. (Cancelled)

21. (Previously added) The semiconductor package of claim 17, wherein the plurality of contacts comprises a plurality of contact pads.

22. (Currently amended) The semiconductor package of claim 21 further comprising a plurality of solder balls attached to said contact pads of said first and second plurality of contacts.

23. (Previously added) The semiconductor package of claim 17 wherein each of the second plurality of contacts is contained within a dimensional profile of an integrated circuit coupled to the top surface of the substrate.

24. (Cancelled)

25. (Previously added) The semiconductor package of claim 17 wherein said top surface of said substrate has a plurality of bond pads.

26. (Previously added) The semiconductor package of claim 25 wherein said top surface of said substrate has a ground bus that is connected to said second plurality of contacts by a plurality of vias that extend through said substrate.

27. (Previously added) The semiconductor package of claim 17 wherein said first plurality of contacts comprises at least five rows of contacts.

28. (Previously added) The semiconductor package of claim 25 wherein said top surface of said substrate has a power bus that is connected to said second plurality of contacts by a plurality of vias that extend through said substrate.

29. (Cancelled)

30. (Currently amended) A semiconductor package, comprising:

a substrate that includes a top surface having a plurality of bond pads, and an exposed external opposite surface [defined by] including an inner region, an outer region, and a middle region that separates the inner and outer regions;

a plurality of contacts including a first plurality of contacts and a second plurality of contacts, said first plurality of contacts located in the outer region, and said second plurality of contacts located in the inner region such that the [first] smallest distances between adjacent contacts in the inner and outer regions

[is different] are smaller than a [second smallest] distance between the inner and outer regions, wherein the middle region is free of contacts; and

an integrated circuit that is mounted to said top surface of said substrate and electrically coupled to said plurality of bond pads, wherein said first and second plurality of contacts are located respectively inside and outside a dimensional profile of said integrated circuit.

31. (Currently amended) The semiconductor package of claim 30, wherein the [first smallest distance is smaller than the second smallest distance] distances between adjacent contacts in the inner region are equal to the distances between adjacent contacts in the outer region.

32. (Cancelled)

33. (Cancelled)

34. (Currently amended) The semiconductor package of claim 30 further comprising a plurality of [solder balls] electrically conductive members attached to said plurality of contacts of said first and second plurality of contacts.

35. (Previously added) The semiconductor package of claim 30 wherein said top surface of said substrate has a ground bus that is coupled to said integrated

circuit and connected to said second plurality of contacts by a plurality of vias that extend through said substrate.

36. (Previously added) The semiconductor package of claim 30 wherein said top surface of said substrate has a power bus that is coupled to said integrated circuit and connected to said second plurality of contacts by a plurality of vias that extend through said substrate.

37. (Currently amended) The semiconductor package of claim 30 [wherein said integrated circuit is enclosed by] <u>further comprising</u> an encapsulant <u>enclosing said integrated circuit</u>.

38. (Cancelled)

39. (Cancelled)

40. (Previously added) An integrated circuit package for an integrated circuit which has a dimensional profile, comprising:

a substrate that includes a top surface, and an exposed external opposite surface defined by a first region that is substantially equal to the dimensional profile of the integrated circuit, a second region, and a third region that separates the first and second regions; and

a plurality of contacts including a first plurality of contacts and a second plurality of contacts, said first plurality of contacts located within the second region, and said second plurality of contacts located in the first region such that a first smallest distance between adjacent contacts in the first region is smaller than a second smallest distance between the first and second regions, said third region being a contact free region.

41. (Previously added) The integrated circuit package of claim 40, wherein a distance between adjacent contacts in first region is the same as the distance between adjacent contacts in the second region.

42. (Previously added) The integrated circuit package of claim 40 further comprising a plurality of solder balls attached to said plurality of contacts.

43. (Previously added) The integrated circuit package of claim 40 wherein said top surface of said substrate has a ground bus that is connected to said second plurality of contacts by a plurality of vias that extend through said substrate.

44. (Previously added) The integrated circuit package of claim 40 wherein said top surface of said substrate has a power bus that is connected to said second plurality of contacts by a plurality of vias that extend through said

substrate.

45. (Currently amended) A [ball grid array] semiconductor package, comprising:

a substrate which has a top surface and an exposed external bottom surface, said external bottom surface having a plurality of contact pads, said plurality of contact pads consisting only of:

an outer array of contact pads, each of said contact[s] pads separated from each other by a first distance;

a center array of contact pads, arranged in a four-by-four array, each of said contact pads separated by a second distance, said center array of contact pads being separated from said outer array of contact pads by a third distance which is larger than said first and second distances; and

a plurality of [solder balls] conductive contacts attached to said contact pads of said [substate] substrate.

46. (Currently amended) The [ball grid array] semiconductor package of claim 45 wherein said outer array of contact pads is located outside an outer dimensional profile of an integrated circuit coupled to the top surface of said substrate.

47. (Currently amended) The [ball grid array] semiconductor package of

claim 45 wherein said center array of contact pads is located inside the outer dimensional profile of an integrated circuit coupled to the top surface of said substrate.

48. (Currently amended) The [ball grid array] semiconductor package of claim 45 wherein said outer array of contact pads is located outside an outer dimensional profile of an integrated circuit coupled to the top surface of said substrate, and wherein said center array of contact pads is located inside the outer dimensional profile of said integrated circuit.

49. (Currently amended) The [ball grid array] semiconductor package of claim 45 wherein a distance between adjacent contact pads in said outer array is the same as the distance between adjacent contact pads in said center array.

50. (Currently amended) The [ball grid array] semiconductor package of claim 45 wherein the smallest distance between adjacent contact pads in the outer array is smaller than the distance between the outer array of contact pads and the center array of contact pads.

51. (Currently amended) The [ball grid array] semiconductor package of claim 45 wherein the top surface of said substrate has a ground bus that is connected to said center array of contact pads by a plurality of vias that extend

through said substrate.

52. (New) The semiconductor package of claim 45 wherein the conductive contacts are solder balls.

53. (New) A semiconductor package, comprising:

a substrate that includes a top surface having a bus and an exposed external opposite surface including a first, inner region, a second, outer region around the inner region, and a third region that separates the first and second regions;

a plurality of contacts including a first plurality of contacts and a second plurality of contacts, said first plurality of contacts located in a four-by-four matrix in the first region, and said second plurality of contacts located in the second region such that a smallest distance between adjacent contacts in both the first and second regions are smaller than a distance between the first and second regions, wherein the third region does not have any contacts located therein; and

a plurality of via interconnecting the first bus with a plurality of the first contacts.

54. (New) The semiconductor package of claim 53 wherein the top surface has a second bus, further comprising a plurality of vias interconnecting the second bus with a plurality of the second contacts.